REMARKS

I. Introduction

With the addition of new claims 31 to 72, claims 1 to 7 and 12 to 72 are currently pending and being considered in the present application, since claims 8 to 11 were previously canceled. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

II. Rejection of Claims 2 to 4 and 6 Under 35 U.S.C. § 112

The claims have been amended herein without prejudice, thereby rendering moot the present rejection. Withdrawal of this indefiniteness rejection of claims 2 to 4 and 6 is therefore respectfully requested.

III. Rejection of Claims 1 to 7 and 12 to 30 Under 35 U.S.C. § 103

Claims 1 to 7 and 12 to 30 were rejected under 35 U.S.C. § 103(a) as assertedly unpatentable in view of the combination of U.S. Patent No. 4,967,340 ("the Dawes reference") and U.S. Patent No . 7,043,416 ("the Lin reference"). The combination of the Dawes and Lin references does not render unpatentable any of the present claims, and the rejection should be withdrawn, for at least the following reasons.

Claim 1 recites coupling at least one unit adapted and an array. The Office Action refers to the CPU 48 of the Dawes reference as assertedly disclosing the at least one unit and to the random access processor 28 and array processor 50 as assertedly disclosing the array.

Claim 1 further provides that the at least one unit comprises an instruction pipeline. Nowhere does the Dawes reference disclose that the CPU 48 includes an instruction pipeline. Indeed, the Office Action refers to the Lin reference as assertedly disclosing a CPU with an instruction pipeline. However, instruction pipelines are generally used for data processing. In the Dawes reference the CPU 48 is not used for data processing. Instead, the CPU 48 is merely used as part of a configuration controller to configure the random access processor 28, which then in turn performs the data processing according to the configuration. There is no suggestion in the cited art to provide an instruction pipeline in a unit that merely provides for configuration of a data processing unit.

Moreover, claim 1 has been amended herein without prejudice to recite that the array is controlled by instructions issued from the instruction pipeline of the at least one

unit to the array. Even if the Dawes references is modified as suggested in the Office Action, the modified system would still not disclose or suggest this feature. The Dawes reference refers to configurations generated based on operator input. Therefore, the Dawes reference does not suggest an embodiment in which an instruction would be issued from an instruction pipeline.

Furthermore, claim 1 has been amended herein without prejudice to recite that the array comprises a packet oriented network. Such a network, it is noted, supports communication between non-next-neighbor cells. For example, a packet may include control information and the data. The Dawes reference, on the other hand, refers only to a next-neighbor type interconnect between cells. The Dawes reference does not refer to an array that comprises a packet-oriented network.

The Lin reference does not correct these critical deficiencies of the Dawes reference. Therefore, the combination of the Dawes and Lin references does not disclose or suggest all of the features of claim 1, and therefore does not render unpatentable claim 1 or any of its dependent claims, e.g., claims 2 to 4, and 12 to 20.

As further regards claim 2, claim 2 provides that at least one data path is provided between the array and the at least one unit and includes a FIFO. The Office Action refers to the Abstract and column 5, lines 27 to 64 of the Dawes reference as assertedly disclosing this feature. However, the cited sections do not refer to memory of any kind between the CPU 48 and the random access processor 28 (referred to by the Office Action as assertedly disclosing the at least one unit and the array, respectively), let alone a FIFO.

The Office Action also refers to the RAM 34 as assertedly disclosing this feature. However, while RAM and a FIFO are both memory, a RAM is not, and does not disclose or suggest use of, a FIFO.

Indeed, any review of the Dawes reference makes plain that it does not at all disclose, or even suggest, a FIFO.

Moreover, as noted in Applicant's previous response, claim 2 provides that the transferring step includes a transfer from the at least one unit to the array ***and vice versa***. In contrast to claim 2, the Dawes reference provides for processing to be performed only by the random access processor 28. The CPU 48 is used merely to configure the random access processor 28. No data is indicated to be transferred from the random access processor 28 to the CPU 48. In the "Response to Arguments" section, the Office Action states that figure 2 shows that elements 28 and 50 communicate with element 48. However, figure 2 clearly shows only a one-way directionality of configuration data from the CPU 48 to the random

access processor 28 (see arrow 55), and does not show data transfer from elements 50 and 28 to the CPU 48 (relied upon by the Office Action as assertedly disclosing the at least one unit). Therefore, the Dawes reference does not disclose transfer from the array to the at least one unit as required by claim 2.

The Lin reference does not correct these additional critical deficiencies of the Dawes reference. For at least these additional reason, the combination of the Dawes and Lin references does not disclose or suggest all of the features of claim 2, and therefore does not render unpatentable claim 2 for these additional reasons.

Claim 5 provides that an array is coupled to by an instruction pipeline of at least one unit, which instruction pipeline controls configurations. As noted above in support of the patentability of claim 1, the combination of the Dawes and Lin references does not disclose or suggest this feature. Therefore the combination of the Dawes and Lin references does not render unpatentable claim 5 or any of its dependent claims 6 and 21 to 28.

Claim 7 provides that an array an at least one unit are coupled, and that the at least one unit includes an instruction pipeline. Claim 7 further provides that the array includes a packet-oriented network communicating values in packets. As noted above in support of the patentability of claim 1, the combination of the Dawes and Lin references does not disclose or suggest these features. Moreover, claim 7 recites "providing a path allowing for block transfer between the array and the at least one unit." Block transfer refers to data is not transmitted merely on a word-by-word basis, but rather by blocks of data words. Such transfer provides for generating a single address for bursting data in a linear address sequence over a bus from the sender to the receiver, whereas word-based data transfer provides memory addresses in each cycle. The Office Action asserts that the Abstract and column 2, lines 2 to 31 of the Dawes reference discloses block data transfer. However, any review of the cited sections makes plain that the cited sections have nothing to do with block-based data transfer. For all of the foregoing reasons, the combination of the Dawes and Lin references does not disclose or suggest all of the features of claim 7, and therefore does not render unpatentable claim 7 or any of its dependent claims, e.g., claims 29 and 30.

Withdrawal of this anticipation rejection of claims 1 to 7 and 12 to 30 is therefore respectfully requested.

IV. New Claims 31 to 72

Claims 31 to 72 have been added herein. Claims 31 to 72 do not add new matter and are supported by the present application, including specification, as originally filed.

Claims 31 to 39 ultimately depend from claim 7 and are therefore allowable for at least the same reasons as claim 7.

Claims 40 to 56 ultimately depend from claim 1 and are therefore allowable for at least the same reasons as claim 1.

Claim 57 provides for coupling at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline, and an array that comprises a plurality of data processing cells having programmable coarse grained ALUs. Claim 57 further provides that the array comprises a packet oriented network communicating values in packets. As noted above, the cited reference do not disclose or suggest these features. Therefore, claim 57 is allowable.

Claims 58 to 72 depend from claim 57 and are therefore allowable for at least the same reasons as claim 57.

V. Conclusion

In light of the foregoing, it is respectfully submitted that all of the presently pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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By: /Aaron Grunberger/
Aaron Grunberger
Reg. No. 59,210

KENYON & KENYON LLP
One Broadway
New York, New York 10004
(212) 425-7200

CUSTOMER NO 26646